

ABSTRACT

*Sub B2*

[0112] A system and method for testing an integrated circuit having internal circuit blocks. Each of the internal circuit blocks may have its own test circuit block, referred to as a socket access port. The integrated circuit preferably includes a chip access port (e.g., an IEEE standard 1149.1 compliant test access port) connected to a set of boundary-scan cells, and connected in a hierarchical fashion to the lower-level test circuit blocks. Each of the lower-level test control circuit blocks preferably comprises a socket access port controller, and test operation is transferred downward and upwards within said hierarchical structure by communicating from a test control circuit block to the test control circuit block at the immediately higher or immediately lower level in the hierarchical structure. Each of the lower-level test control circuit blocks of the hierarchical test control network may be functionally identical. Further, each of the lower-level test control circuit blocks may be structurally identical. An existing boundary scan may be easily modified for use in the hierarchical structure by adding push instructions to send it to a lower-level test circuit block, and pop instructions to return control to the higher level test circuit block.

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